UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/751,747	12/29/2000	Lawrence Henry Hudepohl	MIPS:0105.00US	7128

23669 7590 12/15/2005

HUFFMAN LAW GROUP, P.C.
1832 N. CASCADE AVE.
COLORADO SPRINGS, CO 80907-7449

EXAMINER	
TREAT, WILLIAM M	
ART UNIT	PAPER NUMBER
2181	

DATE MAILED: 12/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/751,747	HUDEPOHL ET AL.	
	Examiner	Art Unit	
	William M. Treat	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 September 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 December 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5/21,7/31,9/17&19,*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 1-23 are presented for examination.

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 10-21 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

4. In each of independent claims 10 and 14, and consequently their dependent claims, applicants claim: "first program code for providing an instruction bus" and "second program code for providing a data bus". The only examples the examiner can think of in which program code provides a bus is either in a simulation or when program code is used to drive chip fabrication. Neither task is consistent with the scope of applicants' original disclosure.

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 10-21 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential elements, such omission amounting to a gap between the elements. See MPEP § 2172.01. The omitted elements are: how program code provides an instruction bus and a data bus.

7. Claims 9, 13, 21, and 23 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

8. As to claims 9, 13, and 21, they claim transferring data in parallel to one or more coprocessors with multiple issue pipelines. It is unclear to the examiner whether applicants are claiming transfer of multiple data elements (language of claim 1) in parallel or merely parallel data lines as opposed to a serial data line.

9. As to claim 23, it is unclear as to how applicants designate "an execution order corresponding to said issuing". If two or more instructions are issued at the same time to a coprocessor, how is the execution order of the two or more instructions determined, and how does it correspond to the parallel issue?

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to

consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

12. Claims 1-9 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Coprocessor Interface (Chapter 10).

13. Coprocessor Interface substantially taught the invention of claim 1 including an interface for transferring data between a central processing unit (CPU) and a coprocessor, the interface comprising: an instruction bus, configured to transfer instructions to the coprocessor in an instruction transfer order, wherein particular instructions direct the coprocessor to transfer the data to/from the CPU (Sections 10.2 and 10.5.1, Fig. 10-1, and Table 10-2); and a data bus, coupled to said instruction bus, configured to transfer the data wherein data order signals within said data bus specify a data transfer order that differs from said instruction transfer order, and wherein said data order signals specify transfer of a data element, said data element corresponding to a specific outstanding instruction wherein said data order is relative to outstanding instructions, said outstanding instructions being those of said particular instructions transferred to said the coprocessor that have not completed a data transfer; wherein the interface keeps track of said data order, and wherein said data order signals indicate said data order, and wherein said data order signals are provided with said data element as said data element is transferred (Sections 10.5.2 and 10.5.3 and Table 10-2, pp. 252 and 253).

14. Coprocessor Interface did not teach interfacing with multiple coprocessors though it did teach being able to interface with two types of coprocessors, a floating

point processor and a graphics processor (Section 10.1, first paragraph). The examiner takes Official Notice of the facts that processors with multiple coprocessors were known in the art at the time of applicants' invention and that improvements in fabrication technology have made it possible to provide a processor and multiple coprocessors in the same amount of chip real estate once consumed by a processor and one coprocessor. One of ordinary skill in the art is motivated to provide a processor with multiple coprocessors to enhance performance through increased parallelism. One of ordinary skill in the art would be motivated to expand the capacity of the Coprocessor Interface to work with multiple coprocessors to provide a system with enhanced performance which permitted transfer of data and instructions in varying order thereby allowing greater flexibility in the use of system bus, etc. resources while still maintaining execution order.

15. As to claim 2, since Coprocessor Interface already taught compatibility with graphics and floating point coprocessors (Section 10.1, first paragraph), it would be logical that it would be used with a plurality of graphics and/or floating point coprocessors thereby increasing overall system performance while minimizing necessary modifications to the interface.

16. As to claims 3-8, this is a claim for how assignee's Coprocessor Interface functioned even before it was applied to multiple coprocessors by applicants (Sections 10.1, 10.2, 10.3, 10.5.1, 10.5.2, 10.5.3).

17. As to claim 9, Coprocessor Interface transfers data in parallel (Figs. 10.2 and 10.3).

18. As to claim 22, it fails to define over rejected claims 1-8.

19. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

20. Claims 10-21 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

21. The computer program of claim 10 seems only to describe an interface, as in written description, and is not executed on a computer nor is it being claimed as an element of a computer-related device.

22. The computer program of claim 14 does not seem to be embodied in a tangible medium nor does the program seem to be executed.

23. The examiner is unable to predict how applicants may choose to modify 10 and 14 to overcome the current rejections. However, applicants should consult the Interim Guidelines for Examination of Patent Applications for Patent Subject Matter Eligibility at the following website: http://www.uspto.gov/web/offices/pac/dapp/ogsheet.html before responding. The last 10 pages are the most relevant when considering a response to the 35 USC 101 rejection.

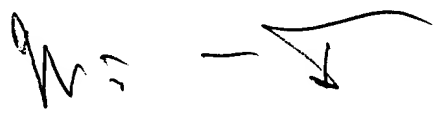
24. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

25. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

26. Any inquiry concerning this communication should be directed to William M. Treat at telephone number (571) 272-4175. The examiner works at home on Wednesdays but may normally be reached on Wednesdays by leaving a voice message using his office phone number. The examiner also works a flexible schedule but may normally be reached in the afternoon and evening on three of the four remaining weekdays.

27. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



WILLIAM M. TREAT
PRIMARY EXAMINER